Rule-based Clock Analysis for Lower Power and Higher Yield at Advanced Process Nodes

Huada Empyrean Software / HiSilicon

ABSTRACT

As technology nodes move into 28nm and below, the SoC design scale and complexity increase rapidly. The clock network has a growing impact on the quality of entire design. Problems on the clock can lead to project delay, chip revision, and loss of yield. Therefore, designers need to consider the clock potential risks as early as possible in the design stages.

As a large scale SoC design company, HiSilicon is committed to optimize clock design and reduce the cost of CTS, in addition to avoid risks. Among them, it is an important goal to improve CTS quality and reduce the power consumption of clock network. The yield is also one of the most concerned indicators. High yield represents high profits, especially in the advanced process. Company annual income will be affected due to yield problems.

This presentation will show you how to perform clock design and yield related analysis in ClockExplorer, a dedicated clock analysis and diagnosis platform, and generate strategies to get better CTS result.

ClockExplorer has integrated many built-in capabilities. For example, for factors that might affect yield, it provides Early Branch OCV, Local Skew, and Physical related checks. It can also display clear clock schematic, analyze clock structure and timing dependency completely, which help designers sort out clock relationships and develop better CTS strategies to achieve lower power cost.

Rule-based Clock Analysis for Lower Power and Higher Yield at Advanced Process Nodes

www.huawei.com

HiSilicon/Empyrean

HUAWEI TECHNOLOGIES CO., LTD.

HUAWEI

HiSilicon SoC Overview

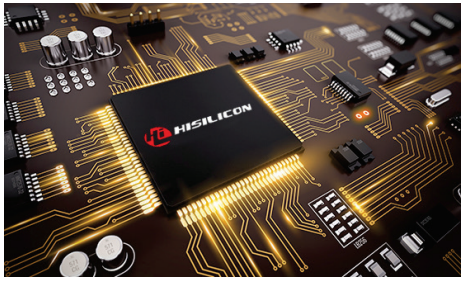
- 17 Years successful R&D experience of SoC chipsets.
- Advanced SoC architecture design & implementation
  - High Performance
  - Low memory bandwidth
  - Low power

Chipset Portfolio

- Infrastructure 
- Cellular Modem 
- Smart Device 
- Home Device 

HiSilicon & Advanced Process Node

- Working closely with TSMC to release multiple chips on advanced process node.
  - N16/N10/N7
- Mature process node flow
  - Process specification
  - PDK & model validation
  - Reference design flow
  - ATE & process diagnostic
  - Mass production control



Clock Impact at Advanced Technology

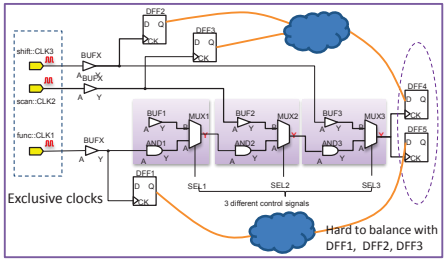
- At advanced process node, the quality of clock network has growing impact on whole project.
  - Project delay
  - Chip revision
  - Loss of yield
- The challenge of building high-performance, low-power system clock trees is also growing.
  - Power consumption & frequency tradeoff
  - Yield problems due to OCV

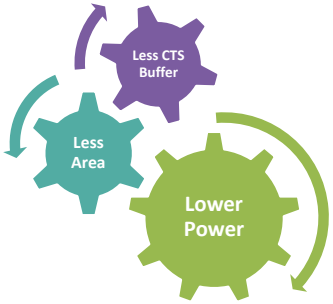
CTS Strategy Challenges

- Bad CTS strategy causes redundant balancing which introduces excessive CTS buffers and leads to high chip density, bad routing and power problems.

Challenges

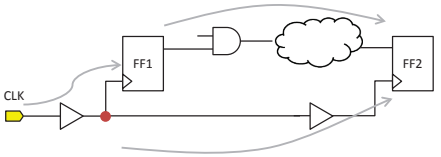
- **Which sink pins need be balanced together?**
- **How to balance for complex mcmm design with mutually exclusive clocks?**





Clock OCV Issue

- **OCV (On Chip Variation)**
  - Cell delay variation
  - Net delay variation



For launch and capture clock paths, the closer from the branch point to root, the greater the probability that the timing will be affected by the variation.

- Under some process, the net delay and cell delay variation between different corners are inconsistent. If the variation trend is different, especially the direction is different, it may cause serious yield issue.

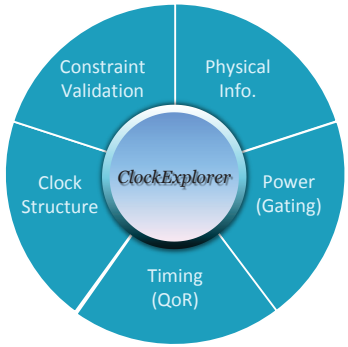
Collaboration with Empyrean

- A customized flow has been built based on *ClockExplorer*[1].
  - Phase I: common discussion on clock analysis platform with Empyrean
  - Phase II: integrate ClockExplorer into reference design flow
  - Phase III: clock diagnosis & CTS strategies generation for better result
- Goals
  - Make better clock strategy
  - Detect OCV issues at early stage

1. ClockExplorer is a clock analysis and optimization platform provided by Huada Empyrean Software Co., Ltd. info@empyrean.com.cn

ClockExplorer: Clock Analysis & Diagnosis

- One-stop checking rule based clock analysis and debugging
- Flexible clock schematic based timing dependency analysis



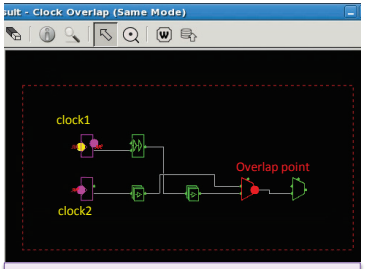
- Shorten CTS Design Cycle
- Reduce Clock Latency
- Reduce Clock Power/Area

Clock Analysis for Better CTS Strategy

Complex Clock Structure Analysis

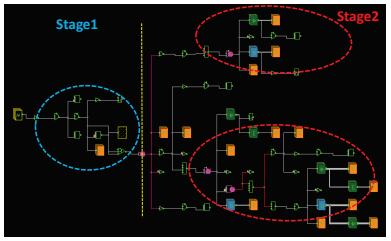
- For a complex clock design, the CTS strategy must be made according to structure analysis and timing dependency analysis.
- Analyze clock structure by inspection rules and clock schematic, separate them into multiple stages and branches to balance.

Inspection rule: clock overlap diagnosis



Step1. balance the tree after overlap point & set don't touch on them.
Step2. balance clock1 and clock2 separately.

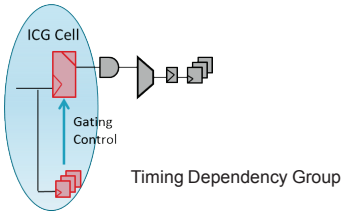
Schematic: clock structure analysis



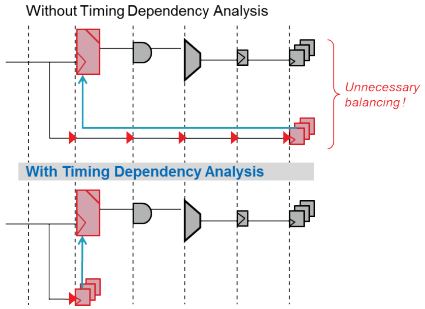
Step1. balance the two branches of stage 2 separately.
Step2. balance stage1.

Timing Dependency Analysis

- Not all flops have timing paths between each other. Only those with timing dependency need be balanced together.
- ClockExplorer provided checking items, analysis commands and schematic operation to show a clear timing dependency picture of entire design.



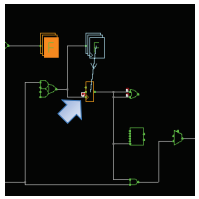
Timing Dependency Group



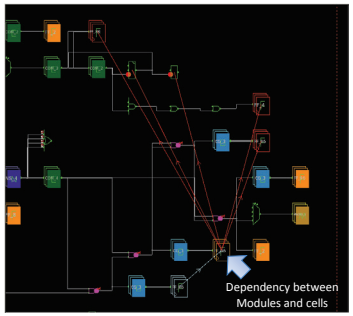
Timing Dependency Connection Display

- The timing dependency analysis can be easily done by "Show Timing Connection" function on schematic.

Flip-flop controls dividers ...

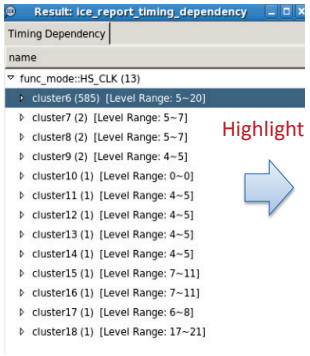


Show timing dependent connections between modules and cells.

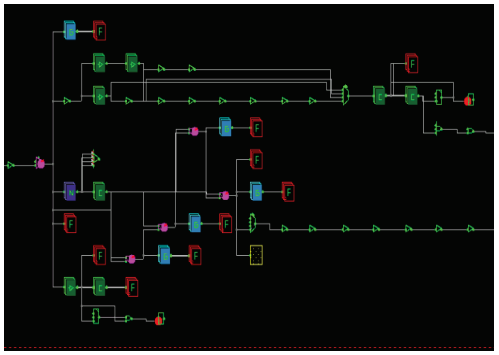


Report Timing Dependency Groups

- Report all clock pins with timing dependency relationships and classify them into different clusters.



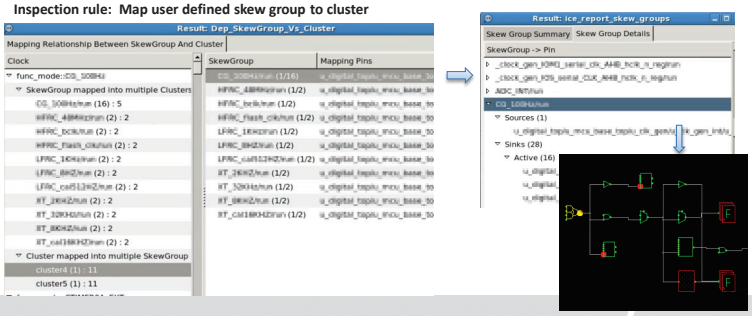
Highlight



User defined Skew Group vs. Timing dependency

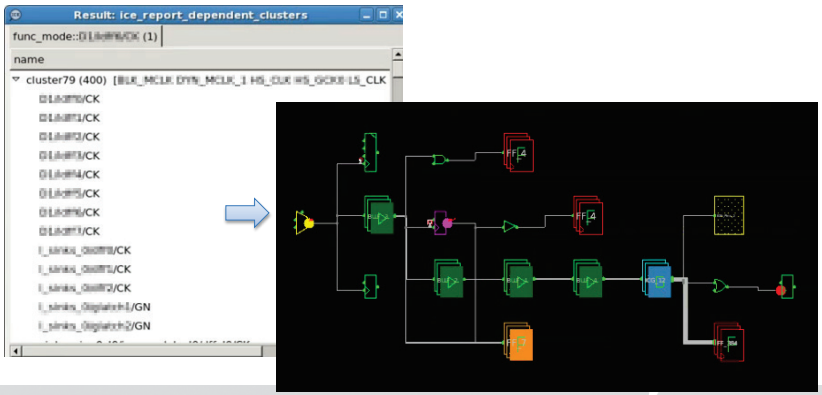
- The skew group definitions in clock spec should be matched with timing dependency clusters.
- Check mapping relationship between user defined skew group and timing dependency cluster
  - If skew group mapped into multiple timing dependency clusters
  - One timing dependency cluster mapped into multiple skew groups

Inspection rule: Map user defined skew group to cluster



Tracing Timing Dependent Pins

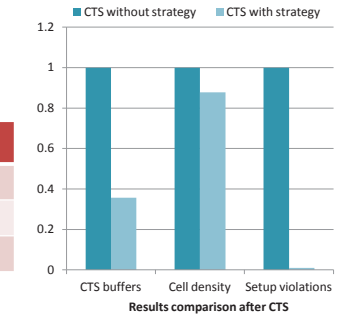
- Trace the timing dependent pins from specified sink pins
- Trace all pins in same skew group from specified sink pin



Successful Story

- Basic Design Information
  - 16nm process mobile design block
  - 3M+ instances
  - 100+ clocks
- Results

	CTS Buffer Count	Cell Density	Routing (H)	Routing (V)
Placement	0	63.99%	0.02%	1%
CTS w/o CE	13191	75.00%	0.09%	4%
CTS w/ CE	4711	65.81%	0.03%	1.5%

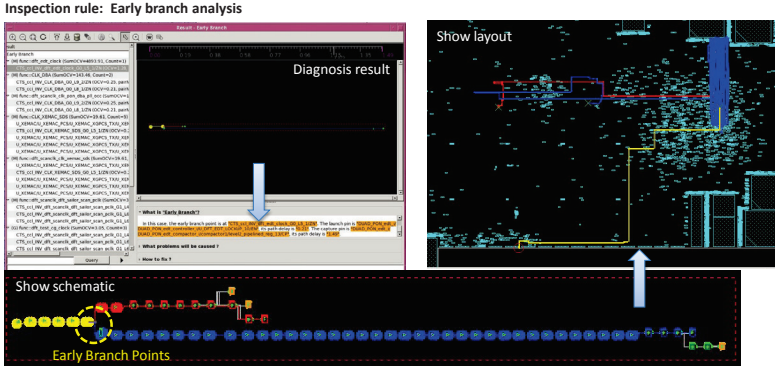


Clock OCV Issue Diagnosis

Early Branch Inspection

- The later the launch and capture paths branched, the less OCV issues.
- Run checking rule of ClockExplorer to catch early branch points of those paths with large local skew.

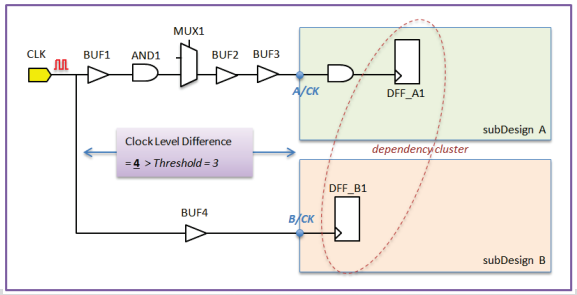
Inspection rule: Early branch analysis



Sub Design Boundary Having Large Level Diff.

- Due to the invisible timing dependency between sub designs, there might be large level difference between the sub design boundaries at top design, which may easily cause timing issues brought by OCV.
- Run checking rule of ClockExplorer to report timing paths crossing physical hierarchy with large clock level differences.

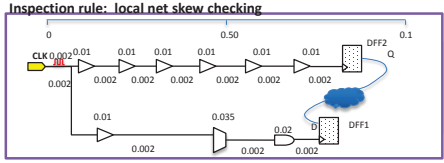
Inspection rule: Sub design boundary having large level difference

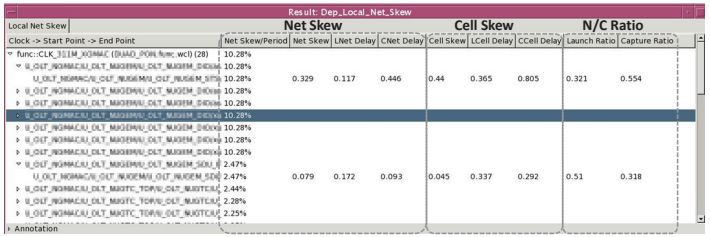


Local Net Skew Diagnosis

- Run checking rule to report the timing paths with large local net skew.
- In different PVT corners, net may have different delay values. Due to OCV effect, large net skew between launch and capture path will cause timing convergence issue, even the local skew is small.

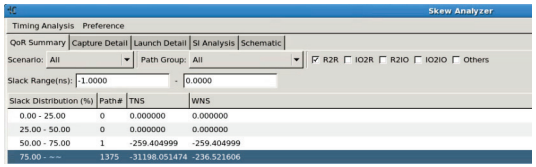
Inspection rule: local net skew checking





Skew OCV Analysis for Violated Paths

- Analyze the violated timing paths according to delay with and without derating.
- Locate those paths which may be easy to be affected by OCV.



Endpoint	Slack	Ocv Common Point	Slack Ocv	L Delay (Derating)	L Delay (No Derating)	L Norm Derate	C Delay (Derating)	C Delay (No Derating)	C Norm Derate	Skew Ocv	Level Diff Clock Paths	Data Ocv	D Delay (Derating)	D Delay (No Derating)	D Norm Derate	Level Data Path
[illegible]	-72.8287	[illegible]	12.1453	414.9000	403.3453	1.0286	14.1749	14.7655	0.9600	1.8538	1	10.2915	356.1552	345.8637	1.0298	3
[illegible]	-74.5488	[illegible]	12.1608	415.9245	404.3476	1.0286	14.0123	14.5961	0.9600	1.8470	1	10.3137	357.1797	346.8660	1.0297	3
[illegible]	-75.5525	[illegible]	12.1991	416.3908	404.7832	1.0287	14.1957	14.7872	0.9600	1.8547	1	10.3444	357.6460	347.3016	1.0298	3
[illegible]	-85.7038	[illegible]	79.3168	2586.7730	2521.5648	1.0259	137.3462	151.4547	0.9068	18.6567	0	60.6600	2418.4568	2357.7968	1.0257	5
[illegible]	-88.3884	[illegible]	79.4421	2589.4577	2524.1240	1.0259	137.3462	151.4547	0.9068	18.6567	0	60.7854	2421.1032	2360.3178	1.0258	5
[illegible]	-98.8462	[illegible]	79.6937	2599.9151	2534.3299	1.0259	137.3462	151.4547	0.9068	18.6567	0	61.0370	2431.5102	2370.4733	1.0257	5
[illegible]	-107.3063	[illegible]	149.8949	4735.3629	4618.6988	1.0253	303.5689	336.7997	0.9013	42.9924	0	106.9026	4381.9661	4275.0635	1.0250	14
[illegible]	-120.0962		0.0000	0.0000	0.0000	1.0000	0.0000	0.0000	1.0000	0.0000	0	51.1177	2443.2567	2392.1390	1.0214	3
[illegible]	-145.2927	[illegible]	138.9235	4338.3530	4222.5821	1.0274	233.7149	256.8676	0.9099	26.5371	0	112.3864	4218.9939	4106.6075	1.0274	17
[illegible]	-147.5792	[illegible]	128.6906	4638.9059	4518.5306	1.0266	79.3268	87.6421	0.9051	12.4392	0	116.2514	4493.1980	4376.9465	1.0266	17
[illegible]	-148.7133	[illegible]	139.0124	4341.7736	4225.9138	1.0274	233.7149	256.8676	0.9099	26.5371	0	112.4753	4222.4145	4109.9392	1.0274	17
[illegible]	-150.8275	[illegible]	139.8720	4343.8877	4227.1684	1.0276	233.7149	256.8676	0.9099	26.5371	0	113.3349	4224.5286	4111.1938	1.0276	16

Summary

- Clock design quality determines the success of chip.
- Hisilicon puts ClockExplorer into the reference design flow to analyze the timing dependent relationship to make better CTS strategies.
- ClockExplorer has integrated many built-in capabilities for yield related check and analysis.
- It helps us to achieve the optimal power consumption and avoid potential issues which may cause yield problem.